



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/730,221	12/05/2000	Andrew C. Walton	10001626-1	9166

22879 7590 06/14/2005

HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER

MANIWANG, JOSEPH R

ART UNIT

PAPER NUMBER

2144

DATE MAILED: 06/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/730,221

Applicant(s)

WALTON ET AL.

Examiner

Joseph R. Maniwang

Art Unit

2144

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12/22/04.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-27 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-27 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 21 December 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119.

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|-----------------------------------------------------------------------------------------|-----------------------------------------------------------------------------|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 102

2. Claims 1-27 are rejected under 35 U.S.C. 102(e) as being anticipated by Marisetty et al. (U.S. Pat. No. 6,675,324), hereinafter referred to as Marisetty.
3. Regarding claims 1 and 12, Marisetty disclosed a method and system comprising (a) reaching a first rendezvous state (see column 7, lines 25-32; column 8, lines 25-35); (b) delaying to allow other cells to reach said initial rendezvous state (see column see column 7, lines 34-37; column 8, lines 40-45); and (c) transitioning to a second rendezvous state (see column 8, lines 60-64); wherein cells of said portion independently execute steps (a) through (c) in parallel (see column 6, lines 23-27). Marisetty further disclosed a processor and a firmware device as claimed (see column 3, lines 53-61).
4. Regarding claims 2 and 20, Marisetty disclosed delaying until all processors coordinated at the first rendezvous state (see column 5, lines 48-53; column 6, lines 22-4, 36-41).
5. Regarding claims 3, 13, and 14, Marisetty disclosed constructing a set of detected cells that have reached a rendezvous state as in response to an error, a group of processors were made to enter an idle state or loop while handling the error, thus

Art Unit: 2144

forming a set of processors in a rendezvous state (see column 5, lines 30-38; column 6, lines 23-27; column 8, lines 6-13). Marisetty disclosed writing such rendezvous sets to memory (see column 6, lines 14-22).

6. Regarding claims 4 and 15, Marisetty implicitly disclosed constructing a global rendezvous set as in response to an error, all but one processors in the system were made to enter an idle state or loop, implying that the all but one processors globally synchronized in an idle state while waiting for the error handling (see column 3, lines 47-52; column 5, lines 30-38).

7. Regarding claims 5, 6, and 16, Marisetty disclosed determining a core cell (monarch processor) from the global rendezvous set for handling the error correction routine and recognizing which processors were effected by the error (see column 5, lines 39-47).

8. Regarding claims 7 and 17, Marisetty disclosed limiting adverse transactions to the other processors by halting their normal operation (see column 5, lines 48-53).

9. Regarding claim 8, Marisetty disclosed the use of an operating system (see column 3, lines 42-46).

10. Regarding claims 9 and 18, the use of complex information to identify cells was inherent in the disclosed ability to identify processors for grouping in a rendezvous set.

11. Regarding claim 10, identification of cells in the rendezvous process could be achieved by the monarch processor (see column 6, lines 7-22).

12. Regarding claims 11 and 19, Marisetty disclosed the use of a cache (see column 4, line 60 through column 5, lines 7).

Art Unit: 2144

13. Regarding claim 21, Marisetty disclosed a method comprising setting a respective register, by each cell, to indicate completion of a subset of boot operations (see column 6, lines 17-22); transitioning to a partition formation state, by each cell, at the earliest of (i) an expiration of a timer, (ii) all cells, within the same partition as indicated in said configuration data, setting their respective registers, and (iii) another cell within the same partition indicating transition to said partition formation state (see column 8, lines 59-64); attempting to determine, by each cell, which other cells belonging to the same partition, have transitioned to said partition formation state to generate a respective local partition set (see column 8, lines 51-64); writing, by each cell, said local partition sets to a globally accessible location (see column 3, lines 47-52); delaying, by each cell, an amount of time after performing said writing (see column 8, lines 40-44); and forming partitions using common information in said local partition sets (see column 8, lines 60-64).

14. Regarding claim 22, Marisetty disclosed resetting cells that are identified as belonging to a partition in said configuration data and that are not identified in common information in said local partition sets (see column 8, lines 58-59).

15. Regarding claim 23, Marisetty disclosed the method wherein a copy of said configuration data is stored on each cell (see column 8, lines 60-62).

16. Regarding claim 24, Marisetty disclosed the method further comprising operating a service processor to update copies of said configuration data on said cells before said transitioning is performed (see column 8, lines 14-20).

Art Unit: 2144

17. Regarding claim 25, Marisetty disclosed the method further comprising analyzing, by each cell, its respective copy of said configuration data to identify data corruption within said copy of configuration data (see column 4, lines 15-36).

18. Regarding claim 26, Marisetty disclosed the method further comprising programming logic coupled to said cells to limit input/output (IO) transactions between cells (see column 5, lines 29-38).

19. Regarding claim 27, Marisetty disclosed the method further comprising initializing a respective operating system on each partition (see column 3, lines 53-61).

Response to Arguments

20. Applicant's arguments filed 12/21/04 have been fully considered but they are not persuasive.

21. Applicant's amendments to the specification and drawings have been entered and are accepted by Examiner. The objections have been withdrawn.

22. Regarding claims 1-20 rejected under 35 U.S.C. 102(e) as being anticipated by Marisetty et al. (U.S. Pat. No. 6,675,324), Applicant asserts that the reference does not teach all limitations of the claims. Specifically, Applicant asserts that Marisetty only involves a single rendezvous state and thus does not disclose transitioning to "a second rendezvous state" as recited in claims 1 and 12. Examiner disagrees. As noted by the Applicant, when an error occurs, an error handling routine begins and causes the system to enter a rendezvous state. Examiner submits that this error handling rendezvous state reads upon the broadly claimed "first rendezvous state". After the

Art Unit: 2144

error is corrected, the processors then transition out of the idle state in response to a "wake up" signal. Examiner submits that moving the processors to this state using a wake up signal reads upon the broadly claimed limitation of "transitioning to a second rendezvous state", as the signal causes all processors to go from an idle state to a state of normal operation.

23. Regarding new claims 21-27, Applicant asserts that Marisetty does not teach or suggest the claimed limitations, such as partitions or transitioning to a partition formation state as claimed. However, Examiner submits that the claimed limitations are taught by the prior art as detailed in the above rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

Art Unit: 2144

the advisory action.' In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph R. Maniwang whose telephone number is (571) 272-3928. The examiner can normally be reached on Mon-Fri 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David A. Wiley can be reached on (571) 272-3923. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JM

MARC D. THOMPSON
MARC THOMPSON
PRIMARY EXAMINER